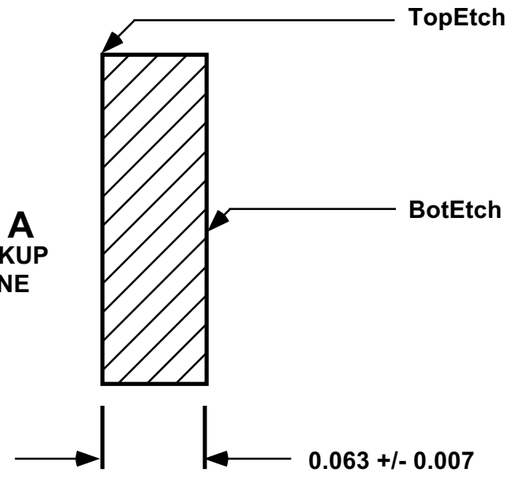
NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: PER IPC-4101/24
   1A. LAMINATE: HIGH-TEMPERATURE FR4
   1B. FINISHED BOARD: .0020 +/-.0005 INCH OUTSIDE LAYERS, COPPER.
   1C. ALL COPPER LAYERS MUST BE SPACED PER DETAIL "A".
   1D. BOARD THICKNESS IS MEASURED INCLUDING TOP AND BOTTOM SIDES FINISHED COPPER. ANY TIN, TIN/LEAD OR GOLD PLATING, SOLDERMASK AND SILKSCREEN LEGEND MUST NOT BE INCLUDED IN FINISHED BOARD THICKNESS.
2. THE CONDUCTOR PATTERN MUST BE ETCHED USING ARTWORK 880011408-003 REV A SUPPLIED WITHIN FABRICATION FILES' ARCHIVE 885011408-003 REV A OR GREATER.
3. ALL CONDUCTOR LAYERS MUST BE REGISTERED WITHIN +/- .005 INCH FROM TRUE POSITION.
4. ETCH TOLERANCES:
   ALL EXTERNAL LAYERS CONDUCTOR WIDTH MUST BE WITHIN +/- .0015 INCH OR +/- 15% OF GERBER DATA, WHICHEVER IS SMALLER.
5. BOARD MUST BE NC DRILLED USING DRILL DATA SUPPLIED.
6. DRILL TOLERANCES AND HOLE SIZES ARE FOR FINISHED BOARD:
   ALL PLATED THROUGH HOLES TO .080 INCH ARE +/- .003 INCH.
   ALL PLATED THROUGH HOLES OVER .081 INCH ARE +/- .005 INCH.
   ALL NON-PLATED THROUGH HOLES ARE +/- .005 INCH.
7. ALL HOLES MUST BE REGISTERED WITHIN +/-.003 INCH FROM TRUE POSITION.
8. MINIMUM ANNULAR RING MUST BE .002 INCH.
9. PLATING:
   9A. PER MIL-C-14550, PLATED THROUGH HOLES MUST BE PLATED WITH .0008 MIN. TO .0015 INCH MAX. THICK COPPER.
   9B. FINISH: IMMERSION GOLD: 2 TO 8 MICROINCHES GOLD OVER 120-240 MICROINCHES OF ELECTROLESS NICKEL.
10. WARP AND TWIST OF FINISHED BOARDS MUST NOT EXCEED .007 INCH PER INCH.
11. SOLDERMASK: PER IPC-SM-840
    11A. SOLDERMASK BOTH TOP AND BOTTOM SIDES.
    11B. SOLDERMASK MUST CLEAR ALL LANDS SHOWN ON GERBER SOLDERMASK LAYERS.
    11C. COLOR GREEN AND SOLVENT FREE.
    11D. LIQUID PHOTO-IMAGEABLE MUST BE .0002 MIN. TO .0008 MAX. INCH THICK MEASURED OVER COPPER PLATING.
12. SILKSCREEN TOP SIDE ONLY USING A GLOSSY WHITE, NONCONDUCTIVE, EPOXY BASED INK. NO SILKSCREEN ALLOWED ON TIN-LEAD OR GOLD AREAS, ON PADS OR IN HOLES.
13. ROUTE BOARD OUTLINE, PER DRAWING DIMENSIONS.
14. VENDOR MUST ENTER VENDOR'S IDENTITY, DATE CODE AND ANY OTHER IDENTIFICATION MARKS AS BOTTOM SIDE SOLDERMASK OPENINGS APPROXIMATELY WHERE SHOWN.
15. OTHER VENDOR NOMENCLATURE OR MARKINGS SHOULD NOT BE ETCHED OR SILKSCREENED ON BOARD WITHOUT PRIOR PERMISSION.
16. ALL VENDOR IN-PROCESS MARKINGS, QA STAMPS, ETC. MUST BE PLACED ON THE BOTTOM SIDE OF BOARD.
17. FINISHED BOARD MUST MEET UL94V-0 RATING AND RoHS COMPLIANCE.
18. DOCUMENTATION THAT MUST BE DELIVERED WITH BOARDS:
    18A. CROSS SECTION REPORT (SPACING BETWEEN COPPER LAYERS AND COPPER THICKNESS)
    18B. ELECTRICAL TEST CERTIFICATION OF COMPLIANCE (ACCORDANCE WITH IPC-ET-652 CLASS II)
    18C. CERTIFICATION OF COMPLIANCE (BOARD HAS BEEN MANUFACTURED TO DRAWING REQUIREMENTS)
    18D. RoHS CERTIFICATE OF COMPLIANCE.

REVISIONS			
REV	DESCRIPTION	DATE	APPD
A	Etch 003 Production Release	01/14/08	

DETAIL A
LAYER STACKUP
SCALE: NONE

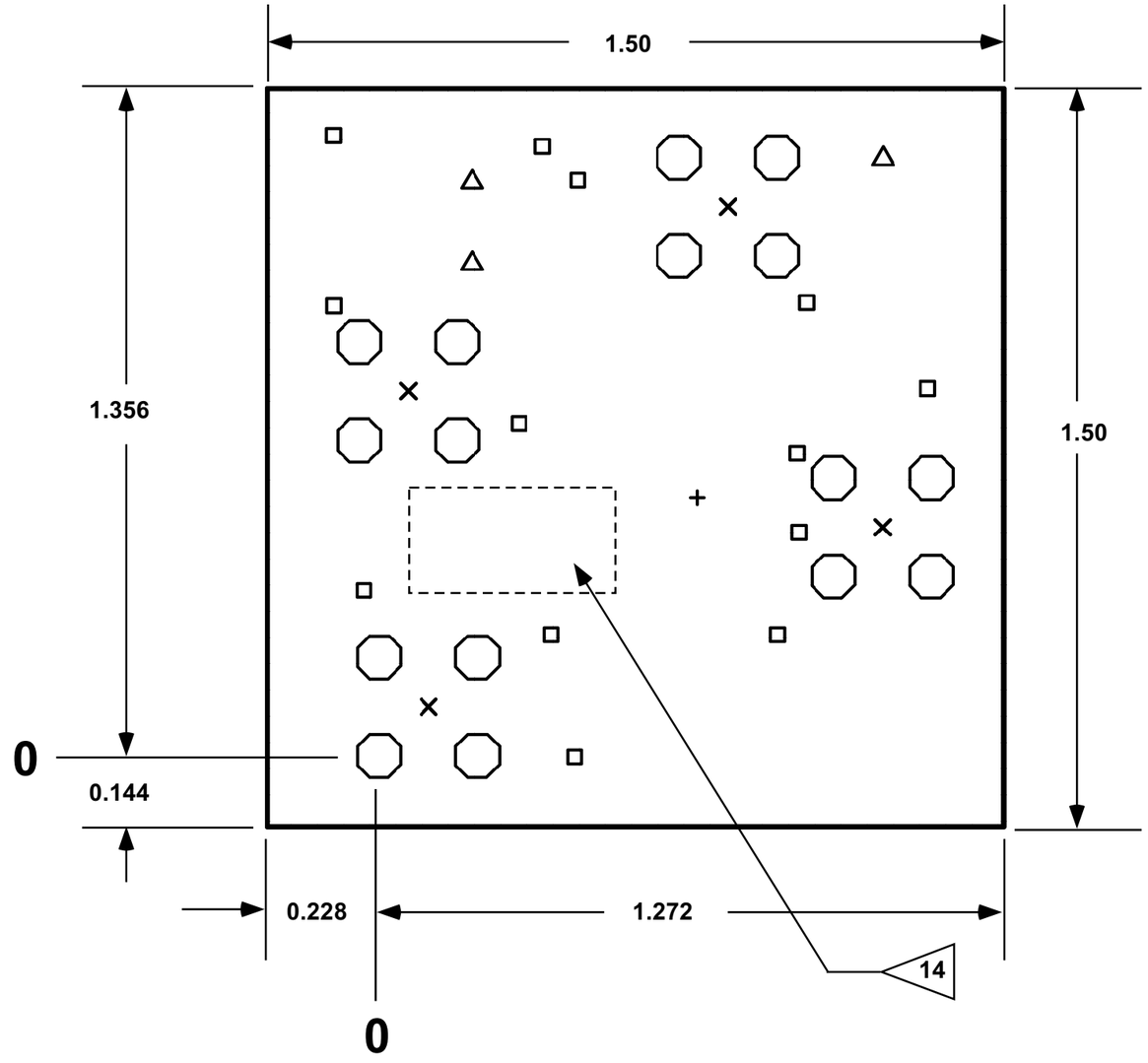


Board Fabrication Information	
	Smallest Feature
Air Gap	.009 inch
Trace Width	.016 inch
Hole Size	.020 inch
Pad Size	.016 x .040 inch
Surface Mount	Top side only

UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE IN INCHES

MATERIAL: SEE NOTES	DRAWN: Ernesto Rey	DATE: 14-Jan-08	National Semiconductor — BOARD & SYSTEM BUSINESS OPERATIONS
FINISH: SEE NOTES	CHECKED:	DATE:	PCB FABRICATION DRAWING LMH730123 Eval
TOLERANCES: 1 PL ± .02; 2 PL ± .01; 3 PL ± .005	ENGINEER: Mary Kao	DATE:	B — DRAWING: 551011408-003 — A
	DO NOT COPY, DISPLAY, OR USE DRAWING WITHOUT AUTHORIZATION DO NOT SCALE DRAWING		SCALE: NONE — SHEET 1 OF 2 — REV

REVISIONS
SEE SHEET #1



DRILL CHART			
ALL UNITS ARE IN INCHES			
SYM	SIZE	PLATED	QTY
+	0.020	YES	1
□	0.028	YES	13
△	0.039	YES	3
×	0.062	YES	4
○	0.067	YES	16

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National Semiconductor™

BOARD & SYSTEM
BUSINESS OPERATIONS

PCB FABRICATION DRAWING
LMH730123 Eval

B	DRAWING: 551011408-003	A
SCALE: NONE	SHEET 2 OF 2	REV